WHAT IS CLAIMED IS:

1. A semiconductor device having a trench isolation layer in a semiconductor substrate, wherein the trench isolation layer comprising a silicon nitride liner, a silicon oxide liner; and a buried layer;

wherein the buried layer includes a first buried layer for filling a lower part of the trench isolation layer and a second buried layer for filling an upper part of the trench isolation layer.

2. The semiconductor device of claim 1, wherein the first buried layer includes an SOG (Spin On Glass) layer.

3. The semiconductor device of claim 1, wherein the second buried layer includes an HDP-CVD (High Density Plasma Chemical Vapor Deposition) oxide layer.

4. The semiconductor device of claim 1, further comprising a silicon oxide layer disposed between the semiconductor substrate and the silicon nitride liner.

5. The semiconductor device of claim 4, wherein the silicon oxide layer includes a thermal oxide layer densified at a temperature over about

800 °C.

6. The semiconductor device of claim 1, wherein the silicon oxide liner includes an HTO(High Temperature Oxide) layer densified at a temperature over 800 °C.

7. The semiconductor device of claim 1, wherein the silicon oxide liner in an upper part of the trench isolation layer is thinner than a lower part of the silicon oxide liner.

8. The semiconductor device of claim 1, wherein an upper surface of the first buried layer is recessed about 1000 Å from the upper surface of the semiconductor substrate.

9. A method of forming a trench isolation layer of a semiconductor device, comprising the steps of:

forming a trench-etching pattern for defining an active area on a substrate;

forming an isolation trench on the substrate using the trench etching pattern as an etching mask;

forming a silicon nitride liner on an inner wall of the trench;

forming a silicon oxide liner on an inner side of the silicon nitride

liner;

performing heat treatment for hardening the silicon oxide liner;

filling the trench having the silicon oxide liner with a first buried layer;

partially recessing an upper surface of the first buried layer by etching; and

filling the trench by depositing the second buried layer on the first buried layer whose upper surface is partially recessed.

10. The method of claim 9, further comprising a step of forming a thermal oxide layer on the inner wall of the trench, between the step of forming the trench and the step of forming the silicon nitride layer.

11. The method of claim 9, wherein the silicon oxide liner includes an HTO oxide layer, and the heat treatment is performed over about 1100 °C for about 30 minutes to about 90 minutes.

12. The method of claim 9, wherein the step of filling the first buried layer includes an SOG layer, and a curing step for changing the SOG layer into a silicon oxide layer is further comprised, before the step of etching the first buried layer.

13. The method of forming the trench isolation layer of claim 12,

wherein the SOG layer includes a polysilazane series material, and the curing step is performed at a temperature of about 700 °C to about 800 °C for about 10 minutes to about 60 minutes.

14. The method of forming the trench isolation layer of claim 9, wherein the step of depositing the second buried layer includes HDP-CVD.

15. The method of forming the trench type isolation layer of claim 9, further comprising the steps of:

exposing an upper part of the trench etching pattern, by removing the second buried layer with a planarization etching; and

selectively removing the trench etching pattern.

16. The method of forming the trench type isolation layer of claim 9, wherein the step of etching the first buried layer is processed by wet etching.